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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/925,952	08/10/2001	Tetsuo Endoh	900-397	5574

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NIXON & VANDERHYE, PC
1100 N GLEBE ROAD
8TH FLOOR
ARLINGTON, VA 22201-4714

EXAMINER	
NGUYEN, JOSEPH H	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/925,952	ENDOH ET AL.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,7-9,11-17,19,29,31-46 and 49-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19,37,38,55 and 56* is/are allowed.

6)☒ Claim(s) *1,3,5,7,8,11,17,18,31-36,39-44,46,49,51 and 53* is/are rejected.

7)☒ Claim(s) *9,12-16,45,52,54 and 57* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5, 7, 8, 11, 17, 18, 31-32, 34-36, 39-41, 43-44, 46, 49, 51 are rejected under 35 U.S.C. 102(b) as being anticipated by Burns Jr, et al. (US 5,990,509).

Regarding claim 1, Burns, Jr. et al. discloses on figures 8 and 10 a semiconductor memory comprising a first conductivity type semiconductor substrate 235; and one or more memory cells comprising an island like semiconductor layer 230, a charge storage layer 265 and a control gate 275, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island like semiconductor layer, wherein an active region of at least one of said memory cells is electrically insulated from the semiconductor substrate by a second conductivity type impurity diffusion layer 215 formed in the semiconductor substrate or in the island like semiconductor layer and means for forming a depletion layer formed at a junction between the second conductivity type impurity diffusion layer 215 and the semiconductor substrate 235 or the island like semiconductor layer 230.

Regarding claim 3, Burns, Jr. et al. discloses on figure 28 a plurality of memory cells are formed with regard to one island like semiconductor layer 230.

Regarding claim 5, Burns, Jr. et al. discloses on figure figures 10 and 28 a semiconductor memory comprising a first conductivity type semiconductor substrate 235; and one or more memory cells comprising an island like semiconductor layer 230, a charge storage layer 265 and a control gate 275, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island like semiconductor layer, wherein an active region of at least one of said memory cells is electrically insulated from the semiconductor substrate; and wherein a plurality of memory cells are formed with regard to one island like semiconductor layer, and the active region of at least one of the memory cells is electrically insulated from another memory cell by: a second conductivity type impurity diffusion layer 405 formed in the semiconductor substrate or in the island like semiconductor layer and means for forming a depletion layer formed at a junction between the second conductivity type impurity diffusion layer 405 and the semiconductor substrate 235 or the island like semiconductor layer 230.

Regarding claim 7, Burns, Jr. et al. discloses on figure 28 a plurality of memory cells are formed with regard to one island like semiconductor layer 230.

Regarding claim 8, Burns, Jr. et al. discloses on figures 10, 13 and 28 a plurality of island like semiconductor layers are formed in matrix, impurity diffusion layers 240 for reading a state of a charge stored in a memory cell are formed in the island like semiconductor layers 230, a plurality of control gates 275 are provided continuously in a direction to form a control gate line and a plurality of the impurity diffusion layers in a direction crossing the control gate line are connected to form a bit line (figure 13).

Regarding claim 11, Burns, Jr. et al. discloses on figure 44 a plurality of memory cells are formed with regard to one island like semiconductor layer 230 and control gates 275 constituting the memory cell are arranged so closely that channel layers of memory cells are electrically connected.

Regarding claim 17, Burns, Jr. et al. discloses on figure 44 a plurality of island like semiconductor layers 230 are formed in matrix, and width (F) of the island like semiconductor layers in one direction is smaller than a distance (F + Δ) between adjacent island like semiconductor layers in the same direction.

Regarding claim 18, Burns, Jr. et al. discloses on figure 44 a plurality of island like semiconductor layers 230 are formed in matrix, and a distance (F) between the island like semiconductor layers in one direction is smaller than a distance(F + Δ) between the island like semiconductor layers in another direction.

Regarding claim 31, Burns, Jr. et al. discloses on figure 10 the impurity diffusion layer 215 is formed in a top portion of the semiconductor substrate 235 immediately under the island like semiconductor layer 230.

Regarding claim 32, Burns, Jr. et al. discloses on figure the island like semiconductor layer 230 is pillar shaped so as to have a height dimension greater than a width dimension.

Regarding claim 34, Burns, Jr. et al. discloses that the semiconductor memory is an EEPROM (col. 6, lines 18-20).

Regarding claim 35, Burns, Jr. et al. discloses on figure 10 said sidewall of the island like semiconductor 230 is vertically extending relative to a surface of the semiconductor substrate 235.

Regarding claim 36, Burns, Jr. et al. discloses on figures 8 and 10 discloses on figures 8 and 10 a semiconductor memory comprising a first conductivity type semiconductor substrate 235; and at least one memory cell comprising an island like semiconductor layer 230, a charge storage layer 265 and a control gate 275, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island like semiconductor layer, wherein an active region of said memory cell is electrically insulated from the semiconductor substrate by a second conductivity type impurity diffusion layer 215 formed in the semiconductor substrate or in the island like semiconductor layer and means for forming a depletion layer formed at a junction between the second conductivity type impurity diffusion layer 215 and the semiconductor substrate 235 or the island like semiconductor layer 230.

Regarding claim 39, Burns, Jr. et al. discloses on figure 10 the control gate 275 and the charge store layer 265 each laterally surround at least said portion of the sidewall of the island like semiconductor layer on all lateral sides thereof.

Regarding claim 40, Burns, Jr. et al. discloses on figure 10 the diffusion layer 215 is formed at a bottom portion of the island like semiconductor layer 230.

Regarding claim 41, Burns, Jr. et al. discloses on figure 10 the island like semiconductor layer 230 is pillar shaped so as to have a height dimension greater than a width dimension.

Regarding claim 43, Burns, Jr. et al. discloses that the semiconductor memory is an EEPROM (col. 6, lines 18-20).

Regarding claim 44, Burns, Jr. et al. discloses on figure 10 said sidewall of the island like semiconductor layer 230 is vertically relative to a surface of the semiconductor substrate 235.

Regarding claim 46, Burns, Jr. et al. discloses on figures 8 and 10 a semiconductor memory comprising a first conductivity type semiconductor substrate 235; and at least memory cell comprising a pillar -shaped semiconductor layer 230 having height dimension greater than a width dimension, a charge storage layer 265 and a control gate 275, wherein the charge storage layer and the control gate entirely or partially surrounds at least a portion of a sidewall of the pillar -shaped semiconductor layer, wherein the sidewall of the pillar-shaped semiconductor layer extends vertically relative to the semiconductor layer; wherein at least a portion of the pillar-shaped semiconductor layer of the memory cell is electrically insulated from the semiconductor substrate by a second conductivity type impurity diffusion layer 215 formed in the semiconductor substrate or in the pillar-shpaed semiconductor layer, and means for forming a depletion layer formed at a junction between the second conductivity type impurity diffusion layer 215 and the semiconductor substrate 235 or the pillar- shaped semiconductor layer 230.

Regarding claim 49, Burns, Jr. et al. discloses on figure 10 the control gate 275 and the charge store layer 265 each laterally surround at least said portion of the sidewall of the pillar-shaped semiconductor layer 230 on all lateral sides thereof.

Regarding claim 51, Burns, Jr. et al. discloses that the semiconductor memory is an EEPROM (col. 6, lines 18-20).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 33, 42 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns, Jr. et al. as applied to claims 1, 36 and 46 above, and further in view of Nishizawa.

Regarding claims 33 and 42, Burns, Jr. et al. discloses on figure 10 substantially all the structure set forth in the claimed invention except the island like semiconductor layer 230 having a circular cross section when viewed from above. Note that the island like semiconductor layer functions as a channel. Nishizawa teaches that the cross section of the channel region may be circular or rectangular (col. 13, lines 5-11). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Burns, Jr. et al. by having the island like semiconductor layer having a circular cross section when viewed from above for the purpose of providing a specific design or application.

Regarding claim 50, Burns, Jr. et al. discloses on figure 10 substantially all the structure set forth in the claimed invention except the pillar shaped semiconductor layer

having a circular cross section when viewed from above. Note that the pillar shaped semiconductor layer 230 functions as a channel. Nishizawa teaches that the cross section of the channel region may be circular or rectangular (col. 13, lines 5-11). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Burns, Jr. et al. by having the island like semiconductor layer having a circular cross section when viewed from above for the purpose of providing a specific design or application.

Claim 53 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burns, Jr. et al. as applied to claim 1 above, and further in view of Derderian.

Regarding claim 53, Burns, Jr. et al. discloses on figure 8 substantially all the structure set forth in the claimed invention except the semiconductor substrate being an SOI board. Note that the semiconductor substrate is a doped semiconductor in figure 8 of Burns, Jr. et al. However, Derderian teaches that the substrate can be SOI or doped semiconductor (col. 4, lines 63-67 and col. 5, lines 1-2). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Burns, Jr. et al by having the semiconductor substrate being an SOI board for the purpose of providing a specific design or application.

Allowable Subject Matter

Claims 9, 12-16, 45, 52, 54 and 57 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 19, 37, 38, 55, 56 are allowed.

The following is an examiner's statement of reasons for allowance:

The reference (s) of record do not teach or suggest, either singularly or in combination at least the limitation of "wherein a lower gate electrode of a first selection transistor, the control gate of the memory cell, and an upper gate electrode of a second selection transistor are arranged in an upward order in a direction vertical to the semiconductor substrate, so that the first and second selection transistors are located opposite vertical sides of the memory cell in a vertical direction so as to sandwich the memory cell therebetween" for claim 19 , "wherein a lower gate electrode of a first selection transistor, the control gates the plurality of memory cells, and an upper gate electrode of a second selection transistor are arranged in an upward order in a direction vertical to the semiconductor substrate, so that the first and second selection transistors are located opposite vertical sides of the plurality of memory cells in a vertical direction so as to sandwich the plurality of memory cells therebetween" for claim 55.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments filed on 14/03/2005 have been fully considered but they are not persuasive.

Applicant argues that in figure 10 of Burns the substrate 235 and the pillar 230 are not electrically isolated by a pn junction, but rather only by the diffusion layer itself, and thus Burns fails to disclose or suggest electrically insulating the pillar 230 from the substrate 235 by a means for forming a depletion layer as recited in claim 1. However, it is inherent that a depletion layer is formed at the pn junction by regions 215 and 235. In figure 10 of Burns, the second conductivity type impurity diffusion layer 215 and the first conductivity type semiconductor substrate 235 are the means that create a PN junction in which a depletion layer is formed. Therefore, Burns discloses means for forming a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306 for regular communications.

JN
April 1, 2005

GEORGE ECKERT
PRIMARY EXAMINER